Visualizing and Quantifying Charge Distributions Correlated to Threshold Voltage Shifts in Lateral Organic Transistors

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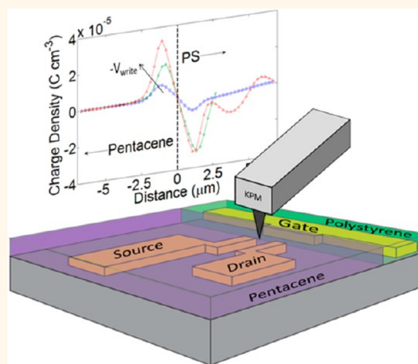
ABSTRACT Lateral organic field-effect transistors (OFETs), consisting of a polystyrene (PS) polymer gate material and a pentacene organic semiconductor (OSC), were electrically polarized from bias stress during operation or in a separate charging step, and investigated with scanning Kelvin probe microscopy (SKPM) and current−voltage determinations. The charge storage inside the polymer was indicated, without any alteration of the OFET, as a surface voltage with SKPM, and correlated to a threshold voltage (V_T) shift in the transistor operation. The SKPM method allows the gate material/OSC interface of the OFET to be visualized and the surface voltage variation between the two gate material interfaces to be mapped. The charge distribution for three samples was derived from the surface voltage maps using Poisson's equation. Charge densities calculated this way agreed with those derived from the V_T shifts and the lateral gate-OSC capacitance. We also compared the behavior of two other polymers with PS: PS accepted the most static charge in its entire volume, poly(2-trifluoromethylstyrene) (F-PS) had the most stability to bias stress, and poly(methyl methacrylate) (PMMA) showed the most leakage current and least consistent response to static charging of the three polymers. This work provides a clear demonstration that surface voltage on a working OFET gate material can be related to the quantity of static charge responsible for bias stress and nonvolatility in OFETs.



KEYWORDS: organic field-effect transistor · scanning Kelvin probe microscopy · static charge · surface voltage · threshold voltage · pentacene · polystyrene

Organic field-effect transistors (OFETs) are an emerging technology that allows for flexible devices with cheaper processing costs for a variety of applications.[1,2] OFETs are now being considered for active matrix backplanes,[3] radiofrequency identification (RFID) tags,[4] and chemical[5] and biological[6] sensing. To design circuits containing OFETs more effectively, the threshold voltage (V_T) should be precisely tuned.[7] Means of shifting V_T include dipolar monolayers[8,9] or chromophores[10] at the OSC−dielectric interface, electrostatic charging of the dielectric,[11] charging of an interface within the gate material,[12] and ferroelectric materials.[13]

An additional V_T shift in OFETs is routinely observed during normal device operation, a phenomenon known as bias stress.[14−21] A major consequence of this phenomenon is poor performance—and ultimately, failure—of circuitry that relies on precisely tuned voltages for operation. The physical origin of this V_T instability has been widely debated in the literature, with agreement on charge trapping as the prevalent mechanism but disagreement on whether mobile charges were being trapped in the OSC or in the dielectric. Recent work by Lee and co-workers[22] has demonstrated the origin of this bias stress to be the buildup of static charge within the material serving as the dielectric at the OSC−material interface, mainly the result of majority carrier drift in the high electric fields subtended across the OFET gate stack. By purposely embedding static charges within the gate material, the influence of the original interfacial potential

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at the OSC−material interface can be usefully superseded, allowing for improved V_T stability and enabling controllable selection of the V_T value for a desired application.[23] These reasons motivate the mapping of interfacial potentials in the OFET to identify static charge trapped in the gate material.

In the conventional ("vertical") device geometry, the gate dielectric is very difficult to probe without altering one of the layers. On the other hand, when using a lateral architecture, an edge of the gate dielectric/OSC interface is exposed, allowing for direct measurements across the interface and along one face of the bulk dielectric. Previous work with lateral transistors did not allow for imaging of the gate dielectric/OSC interface.[24] In this work, we visualize the charge stored at the interface between an OSC and a gate material for the first time, using pentacene as semiconductor and polystyrene, poly(2-trifluoromethylstyrene), and poly(methyl methacrylate) (PS, F-PS, and PMMA, respectively) as gate materials. The charge was imaged under ambient conditions using Scanning Kelvin Probe Microscopy (SKPM) as described in our previous work.[25,26] This imaging technique offers insight into the operation of OFETs where charge is stored inside the gate material layer, and has been used to study the role of water in bias stress at an SiO_2 interface[27] and the static charging of an OSC single crystal.[28] More specifically, we show in this study that the quantity of stored charge in the PS calculated from a Poisson's equation treatment of the SKPM data is of the same quantitative order as the charge that should have led to the V_T shifts, based on the lateral capacitance of the region between the gate and OSC. This is the first *in situ* observation of stored static charge related to V_T shifts in OFETs, providing direct experimental evidence of charge carrier drift from the OSC into the gate material and furnishing a needed example of the correlation of SKPM measurements with independent parameter determinations.[29]

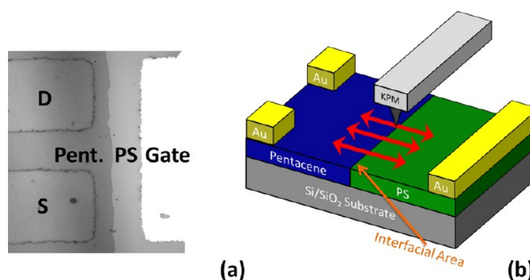


Figure 1. (a) An optical microscope picture of the lateral OFET. Note that the distance between source and drain electrodes is 30 μm and the distance between the source/drain and gate electrodes is 30 μm. About half ($\pm$ a quarter) of the source/drain to gate distance is taken by the PS region. (b) Schematic of the SKPM scanning direction "*x*", parallel to the double arrows.

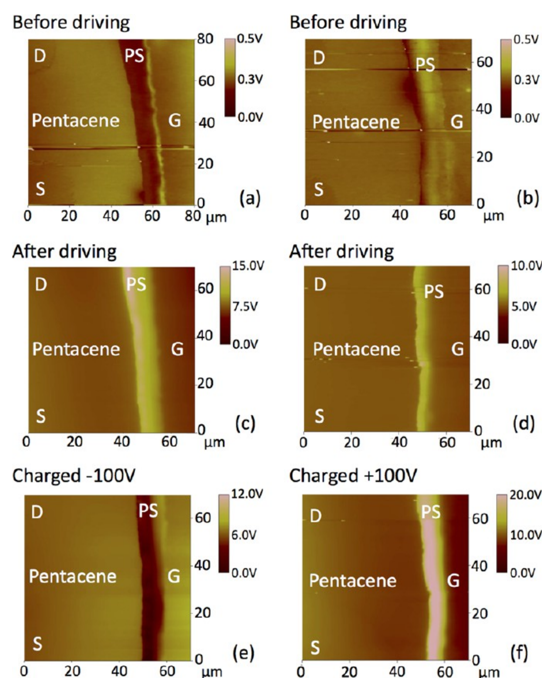


Figure 2. SKPM surface potential scans of lateral PS transistors. The source and drain electrodes, though difficult to see, are always at the left of the image and the gate is at the far right. The pentacene is on the left and the PS on the right of the interface. Images (a, c, and e) and (b, d, and f) correspond to individual samples. The samples are first imaged before electrical testing (a and b). After the transistor electrical measurements, the samples are scanned (c and d). The samples were then charged to −100 V (e) and +100 V (f) for 10 min and rescanned. The correspond height scans can be seen in the Supporting Information Figure S2.

RESULTS AND DISCUSSION

Lateral PS OFET Measurements. The lateral OFETs (Figure 1a, made as shown in Supporting Information Figure S1) were imaged with the SKPM (Figure 1b) under ambient conditions at three different stages: before the transistor electrical measurements were performed, after the transistor electrical measurements were performed, and after charging the gate material.

The SKPM images shown in Figure 2 are of two separate PS samples at the three stages of measurements, following height scans as shown in Supporting Information Figure S2. All measurements were performed with no electrical contacts to the transistors, *i.e.*, the devices were left floating. The samples were removed from the SKPM between scans, resulting in slight changes in orientation for each scan. The first scan was performed on the pristine lateral OFET before any transistor measurements were made, the second scan was performed after the transistor was electrically tested, and the final SKPM scan was of a 'charged' lateral OFET. Additional sample SKPM scans can be seen in the Supporting Information (Figure S3). The initial surface potential difference is small, on the order of a few hundred millivolts, but after transistor operation, the PS displayed a much more positive surface potential than the pentacene side, of roughly 3−5 V. The static charge, a form of "bias stress" in this sample, is concentrated at the semiconductor/gate material

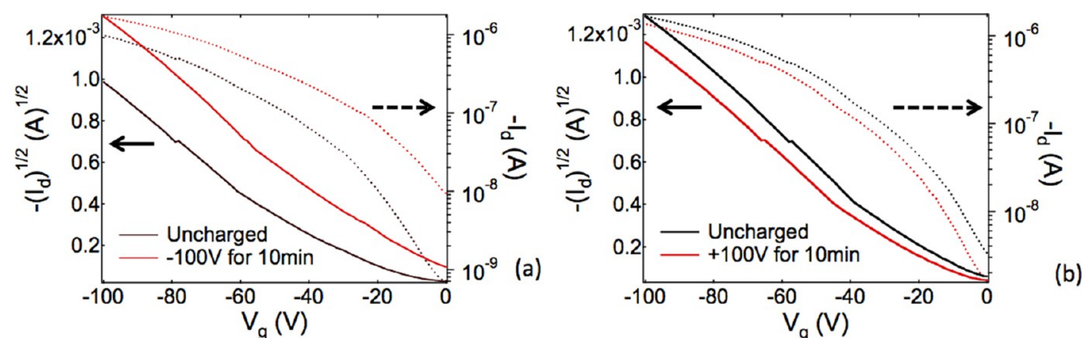


Figure 3. Transfer curves for the samples shown in Figure 2. The black curves were obtained before the samples are charged, while the red curves were from samples after charging. The dashed line corresponds to the log scale, while the solid line is the square root of the drain current. The samples were charged to −100 V (a) and +100 V (b).

interface with less charge apparent closer to the gate electrode. Note that it *is not possible to visualize charge distribution between the gate electrode and OSC in the usual vertical architecture, but with our lateral architecture, such evaluations are possible on unaltered OFETs.* The change in surface potential is due to the accumulation and trapping of the positive charge carriers inside the PS gate material layer from the channel of holes being transported from source to drain. This trapping was seen with all the samples tested and can be related to earlier results that show the positive charge carriers altering the surface potential by becoming trapped in a hexamethyldisilazane-modified SiO_2 gate layer.[8,14] This gate biasing effect has been studied in great detail and is one of the major remaining hurdles in commercialization of OSCs.

When the sample is intentionally charged, this surface potential difference between the PS and pentacene can be increased, as in the case of positive charging from the source and drain, or it can be reversed and the surface potential can be made more negative, as in the case of negative charging. In virtually all cases, 10 min of charging resulted in a shift in PS surface potential in the charging direction. Note that the interelectrode distances in these devices are higher (and less easily controlled) than typical for vertical OFETs, so the operational voltages are high as well. However, the fields created by our voltages, if established in vertical OFETs with typical fabrication dimensions, would correspond to applications of the order of 1 V.

Transistor electrical measurements were performed before and after charging, which was conducted under conventional fluorescent laboratory lighting. The threshold voltage V_T was obtained by plotting the square root of the drain current I_d *vs* gate voltage V_g (Figure 3) and linearly extrapolating the curve between $V_g = -60$ V and -100 V to zero current, an arbitrary but objective definition. Negative charging resulted in positive V_T shifts, meaning the device was easier to turn on, while positive charging resulted in negative V_T shifts, making the device harder to turn on. The positive charging can be considered as a prolonged accumulation biasing, with more positive charges injected into the PS from the pentacene. Figure 3 shows transfer curves for the two samples from Figure 2 before and after charging. Corresponding output curves are shown in Figure 4. When the devices were positively charged, the on/off ratio increased, while negative charging resulted in lowered on/off ratios. Leakage current varied by device and was approximately 10% of source-drain current. Note that only a fraction of the applied charging voltage drops across the PS−pentacene interface because of the PS series resistance, and this fraction also varied from sample to sample because of the limited precision with which the interface can be positioned between the gate and source-drain electrodes.

The observation that both positive (accumulation) and negative (depletion) charging results in noticeable V_T shifts as seen in Figure 3 suggests that a transfer of both holes and electrons from the pentacene layer into the PS are possible. These data are consistent with measurements reported by Podzorov and Gershenson[21] for single-crystal rubrene OFETs, where a similar shift in the onset voltage was associated with photogenerated carriers drifting into a perylene material during charging in the presence of illumination. The asymmetry of the V_T shift in our pentacene OFETs for equal charging voltages as shown in Figure 3 is also qualitatively similar to that of Podzorov and Gershenson, with depletion voltages resulting in larger ΔV_T than accumulation voltages. Given these data and the presence of ambient lighting during our charging experiments, the observed V_T shifts could have been partly the result of photoassisted implantation of photogenerated carriers, However, additional experiments that we had described in ref 26 showed fairly analogous polystyrene interface charging behavior whether the interface was polystyrene−pentacene or polystyrene−gold, suggesting that photoactivation of carriers in the pentacene would not be a requirement for charging.

Individual lateral OFETs were charged to varying voltages ranging from ±25 to ±125 V. Generally, negative charging gave a greater shift in V_T compared to positive

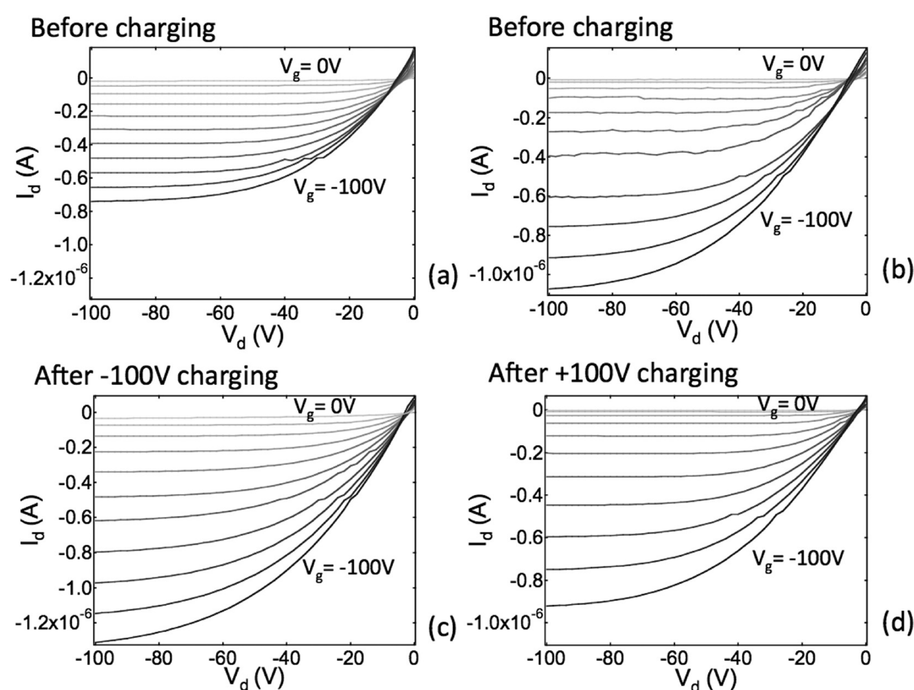


Figure 4. Output curves for the transistors in Figure 2, before (a) and after (c) −100 V charging and before (b) and after (d) +100 V charging. Note the slightly different *y*-axes. The gate voltage was stepped from 0 V to −100 V in −10 V increments.

charging, but the directions of V_T shift were nearly always consistent with the charging voltage signs. We have previously shown that the negative charging results in greater shifts in surface potential, thus having greater influence on V_T.[26] Figure S4 (Supporting Information) shows the dependence of V_T on the charging voltage. For charging voltages between −25 and −90 V, the V_T shifts and charging voltages are correlated, while because of the previously discussed lower stability of injected positive charges, positive charging voltages are not correlated, except by sign, with V_T shifts. At voltages with magnitudes above 100 V, there is the possibility of breakdown and we see that some lateral OFETs show signs of degradation, resulting in smaller V_T shifts. The thickness of the gate material layer (the distance from the gate electrode to the OSC/material interface) varies from device to device, as mentioned above, which will also add uncertainty to the total charge stored in the gate material layer.

Quantitative Relationship between SKPM-Derived and V_T-Shift-Derived Charge Densities. The surface potential scans acquired with SKPM afford the opportunity to quantify the charge trapped in the PS layer after electrostatic charging. As each linescan along the scan direction x (Figure 1) measures the surface potential $V(x)$, changes in the surface potential along the scan direction can be understood within the framework of Poisson's equation,

$$\frac{\partial^2}{\partial x^2} V_s(x) = -\frac{\rho_s}{\varepsilon \varepsilon_0} \quad (1)$$

where $V_s(x)$ is the surface potential, ρ_s is the charge density at the surface of the material, ε is the dielectric constant, and ε_0 is the permittivity of free space. By taking the Laplacian of the surface potential, the surface charge of the PS layer can be estimated numerically, as discussed in the Methods section.

As discussed in the Supporting Information, the pentacene near the PS interface exhibits a sharp topographical feature, the result of the fabrication process. To estimate the location of the actual PS interface (and not this ridge), surface profile plots were created using a contouring algorithm.[30] The main topographical features of the plots were created by extracting the features with the largest area density in each image (see Methods). The PS−pentacene interface was determined to be at the edge of multiple closely spaced contour lines of constant height taken near the expected PS−pentacene interface location. Contour lines become closely spaced at the edge of sharply rising features. The location of this extra PS edge is roughly 1−2 μm left of the highlighted interface, as shown in Figure 5.

Surface charge density (ρ_s) plots were also created using the same contouring algorithm and the results of the Poisson's equation analysis. To illustrate changes in charge density as a function of driving and charging time, surface charge density plots were overlaid onto height profile plots captured during the same scan as the surface potential images. Figure 6 shows the surface charge density ρ_s overlaid onto the height profile for the OFETs illustrated in Figure 2. To distinguish surface profile features from charge density features, all surface profile features are traced in black, while all ρ_s features are traced in color. The three frames in Figure 6 correspond to the calculated ρ_s in the lateral

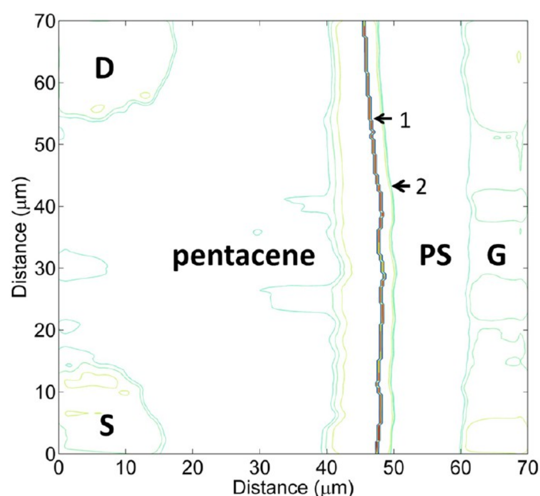


Figure 5. Illustration of height profile contour of the OFET shown in Figure 2 of the main text. The line indicated by number 1 corresponds to the sharp ridge at the PS–pentacene interface indicated by the height scan. The line indicated by number 2 corresponds to the edge of the PS–pentacene interface as approximated by the contouring algorithm.

OFET before driving, after driving, and after charging at −100 V for 10 min, respectively. The physical orientation is the same as for all other images in this paper. The colored contours correspond to areas of constant and high charge density, as scaled by the colorbar on the right of each image. The black and gray contours correspond to the physical features of the surface, similar to the profile illustrated in Figure 5.

Comparison to V_T Data. We can calculate the change in charge density at the PS–pentacene interface that results from OFET charging from the data in Figure 6. Before driving, the charge density derived from the Poisson's equation analysis at the PS–pentacene interface is roughly 10 μC cm^{-3} positioned about 2–3 μm perpendicular to the interface (in the x direction) on the pentacene side. We can integrate the volumetric charge density illustrated in Figure 6b along the x-direction over a range of 2.73 μm into the pentacene layer, changing the units from coulombs to electron charges, yielding an interfacial positive charge density $\sigma = 9.7 \times 10^9$ cm^{-2}, where the area units refer to the cross-sectional interfacial area shown in Figure 1. Much of this charge is compensated by apparent negative charges dispersed elsewhere in the pentacene. By comparison, after charging at −100 V for 10 min, the peak charge density increases to 30–40 μC cm^{-3} over the same spatial extent, and integration of Figure 6b yields a value of $\sigma = 2.5 \times 10^{10}$ cm^{-2}, with little apparent compensating charge in the pentacene.

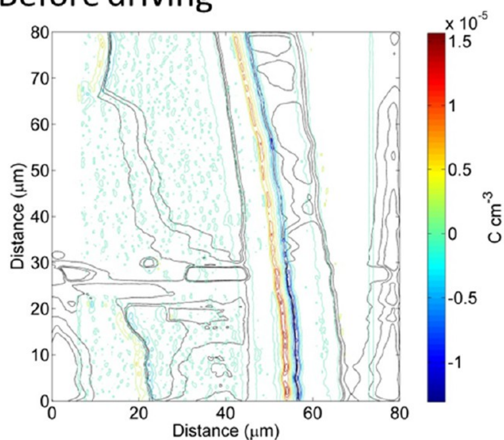
To assess whether this change in interfacial charge density is consistent with the observed V_T shifts, we employ a common estimate for the areal charge density at the semiconductor–polymer interface in an OFET as a function of threshold voltage shift, given by the simple relation

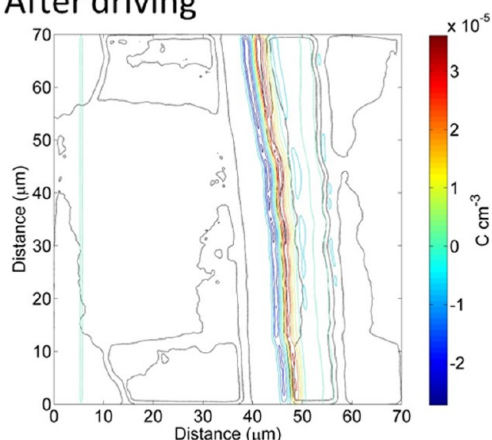
$$\sigma_{cap} = \frac{C_i}{e}\Delta V_T \qquad (2)$$

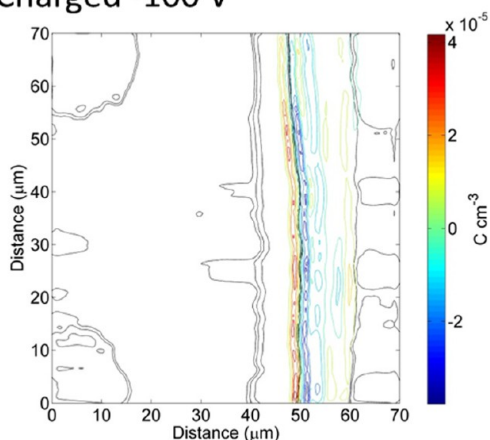
where e is the fundamental charge, ΔV_T is the threshold voltage change $|V_T - V_{T,0}|$, σ_{cap} is the resulting interfacial charge density, and $C_i = \varepsilon\varepsilon_0/t_i$ is the specific capacitance of the polymerlayer—again keeping in mind that the "area" of the capacitor is the interfacial area and the "thickness" t_i of the gate material layer is in the x direction parallel to the substrate (refer again to Figure 1). For the transistor that had been charged to −100 V, the "gate material thickness" is approximately 7.6 ± 0.9 μm, corresponding to a specific capacitance of ~0.30 nF cm^{-2}, and the value of ΔV_T is −18 V. Substituting these values into eq 2 and again working in units of electron charge yields $\sigma_{cap} = 3.4 \times 10^{10}$ cm^{-2} for the charged device, in good agreement with the Poisson's equation analysis discussed above, each value within 15–20% of 3.0×10^{10} cm^{-2}.

We examined two of our other samples at this level of detail, one charged at −50 V and one at −75 V (Figure 7). Because the plots from all three charging values use identical contours spaced between −60 and 60 μC cm^{-3}, the differences in absolute charge density near the PS–pentacene interface are readily observed, revealing a clear increase in ρ_s with increasing charging voltage. A comparison between the charge density calculated from the two methods discussed above is shown in Table 1. For the −50 V charged OFET, the values calculated from both methods—σ_{SKPM} and σ_{cap}—differ by less than 15% from the average of the two. Considering the numerous uncertainties in defining the positions of charges and interfaces, and the possibility of static charge arising from impurities, this agreement is remarkable. The third sample was an OFET charged to −75 V that also happened to have a much lower "gate material thickness". In this case, the much thinner gate material results in a higher estimate of the charge from eq 2 as compared to the integrated charge density ρ_s. Some of the negative charge in the PS layer at the PS–pentacene interface is likely compensated or screened by positive charge injected from the [opposite] PS-Au interface, resulting in a lower charge density on the pentacene side than the capacitor approximation would predict. The thinner material might have also been more generally unstable to this level of charging voltage.

As illustrated in Table 1 and discussed above regarding Figure S4, OFETs subjected to increasingly greater charging voltages generally displayed greater ΔV_T, the result of the V_T shifts being associated with greater charge accumulated in the semiconductor channel. This charge density is of the same order







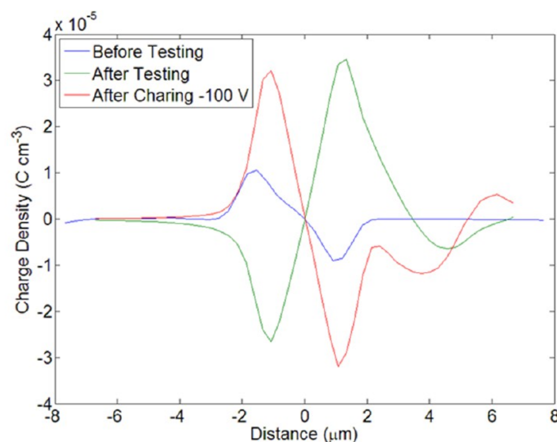
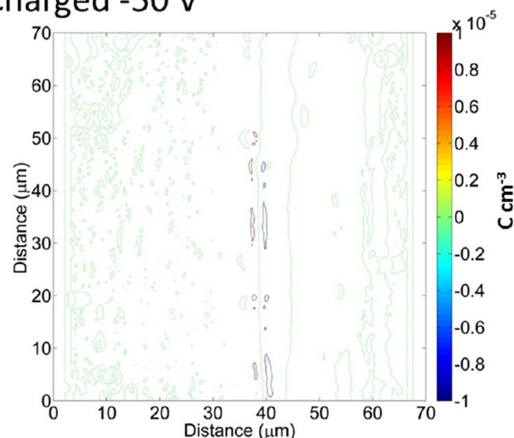
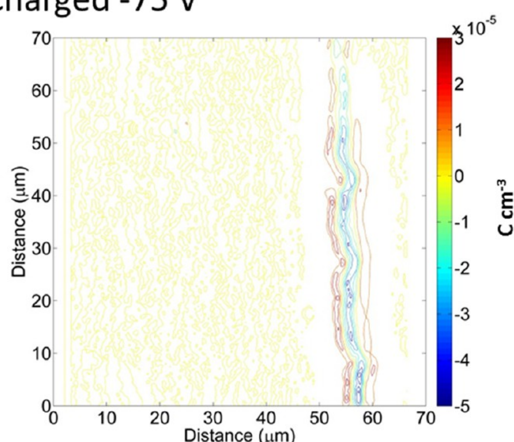


Figure 6. (a) Charge Density maps of an OFET from Figure 2. Before driving, the device shows a small amount of charge at the PS−pentacene interface, consistent with its surface potential plot. Before driving, the PS near the pentacene interface is more negative than the adjacent pentacene layer. After driving, the PS at the interface becomes more positive than the pentacene, the result of driving holes into the PS layer. Upon charging to −100 V for 10 min, the PS layer is more negative than the adjacent pentacene layer, and has significant charge extending into the PS . (b) Corresponding cross section of charge density illustrated in (a).

of magnitude (10^{10} cm^{-2}, from integrating the curves on the pentacene side) as the negative charge density in the PS, with the 50 V charging giving 5×10^9 cm^{-2}, in excellent agreement with σ_{cap}. In addition, the −100 V device showed greater total negative charge on the PS side (including the region farther from the interface) than the −75 V sample, as would be expected.

To investigate the dependence of stability and chargeability on the gate material structure, we used F-PS and PMMA instead of PS. Previous studies have shown that fluorinated dielectrics help prevent





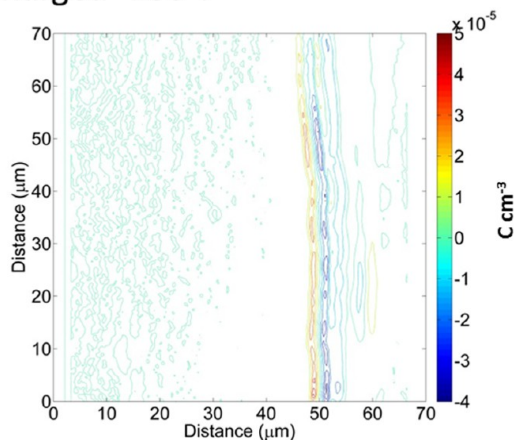


Figure 7. Comparison of charge density distribution for OFETs charged to −50 V, −75 V, and −100 V, respectively. All images have been contoured using 13 levels, spaced in 10 μC cm^{-3} increments from −60 to 60 μC cm^{-3}.

bias stress.[31] Figure 9 shows SKPM scans for the F-PS system; note that unlike the PS sample, the charge stored inside the F-PS after transistor operation did not penetrate nearly as deeply, and is of a much lower magnitude. This observation is consistent with the model developed by Lee and co-workers,[22] in which the gate material charging is the result of charge transfer from the OSC highest-occupied molecular orbitals (HOMO) into localized tail states in the gate material. The lower HOMO of fluorinated polymers such as F-PS as compared to PS would result in tail states with a greater energy offset from the pentacene HOMO, leading to reduced gate material charging.

TABLE 1. Geometric and Electrostatic Parameters for Charged OFETs[a]

charging voltage	t_i (μm)	C_i (nF cm^{-2})	ΔV_t (V)	σ_{SKPM} (cm^{-2})	σ_{cap} (cm^{-2})
-50 V	14.2 ± 0.9	0.16	5.3 V	6.8×10^{9}	5.3×10^{9}
-75 V	2.3 ± 0.4	1.00	15.9 V	1.5×10^{10}	9.9×10^{10}
-100 V	7.6 ± 0.8	0.30	18.0 V	2.5×10^{10}	3.4×10^{10}

[a] t_i is the material thickness, C_i is the material specific capacitance, ΔV_t is the threshold voltage shift, σ_{SKPM} is the charge density estimated from the Poisson analysis of the pentacene-side charging and σ_{cap} is the charge density estimated from the capacitor approximation. The charge density derived from SKPM data is the charge density integrated on the pentacene side within 2.73 μm from the PS—pentacene interface, as shown in Figure 8.

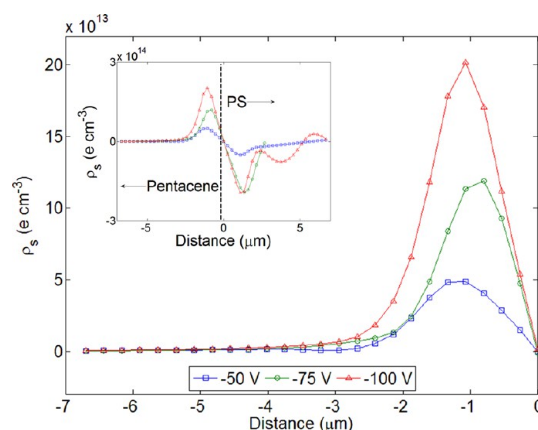


Figure 8. Charge density on the pentacene side, and (inset) across the PS—pentacene interface in each charged OFET (median of 256 linescans per OFET). The increase in accumulated positive charge density in the pentacene layer with increasing charging voltage is consistent with the observed V_t shift for these OFETs.

PMMA lateral OFET images are shown in Figure S6. The surface potential of the PMMA region closest to the pentacene was more positive after device operation and could be made more positive with positive charging and more negative with negative charging, just as with the polystyrenes. However, the PMMA devices exhibited much greater leakage currents (in some cases close to 1/3 the I_d, where leakage current is defined as the current from the gate to the source electrode) than either the PS or F-PS. PMMA showed less capacity to store static charge and also gave less consistent device currents and changes in response to charging of particular signs relative to PS, as could be expected from the greater polarity of PMMA. Other work has shown that the increased polarity of PMMA over PS increases the energetic disorder at the interface.[32] It has also been shown that hydrophobic

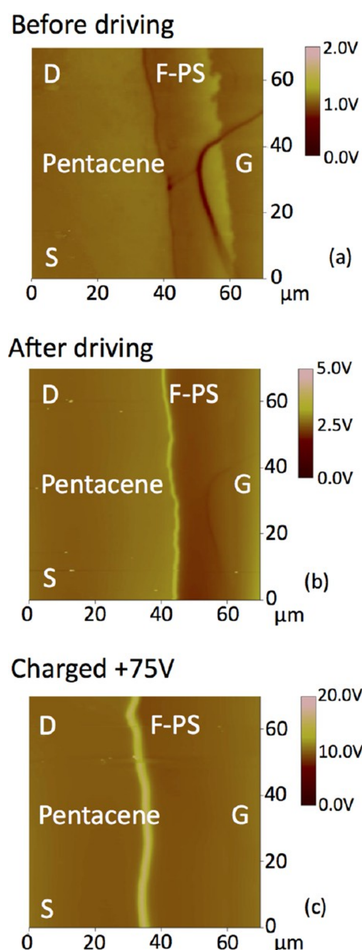


Figure 9. SKPM surface potential scans of the F-PS lateral transistors. The interface has the pentacene on the left and the F-PS on the right. The electrodes are oriented in the same manner as Figure 2. (a) The samples are first imaged before electrical testing. (b) After the transistor electrical measurements, the samples are scanned. (c) The sample was then charged to a value of +75 V (f) for 10 min and rescanned. The corresponding height scan can be seen in the Supporting Information Figure S5.

and nonpolar materials like PS help increase the nonvolatile memory performance of OFETs.[33]

To compare the bias stress behavior of the PS and F-PS transistors, we prepared conventional 'vertical' devices with and without precharged gate materials (see Supporting Information and Figure S7 for procedure and additional data). The uncharged F-PS showed a greatly improved resistance to bias stress compared to PS (Figure 10), while charging greatly improved PS bias stress resistance to a level at least as good as F-PS at short times, pointing to a means of improving bias stress stability in a polymer that might have other desirable attributes such as processability or surface functionality. Charging had little effect on F-PS bias stress at short times and may have been detrimental at long times, possibly suggesting a change in the energy offset between the pentacene HOMO and the F-PS tail states as a result of partially filling the F-PS tail band.[22]

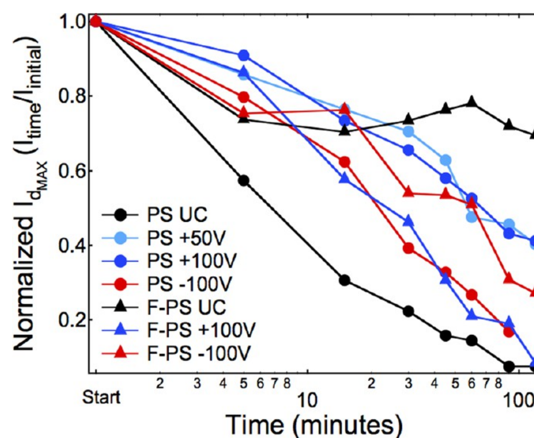


Figure 10. Bias stress behavior of PS (circles) and F-PS (triangles) OFETs. The level of positive charge in the PS samples did not seem to change the gate bias behavior of the OFETs. Positive charging helped the PS sample more than the F-PS. The F-PS performed best with no charging.

In addition to the PS, F-PS, and PMMA gate materials, we also investigated lateral "control" OFETs with an air gap gate (omitting the PS/F-PS). Output curves from some no-PS devices before and after charging are shown in Figure 11. Although the air gap did lower the leakage current to sub-nanoampere levels, these control devices showed poorer on/off ratios, field effect over a more limited range, no saturation behavior, and different V_T shifts from charging. These data offer clear evidence that the PS or F-PS, when present, is the principal gate material in these kinds of devices. After negative charging, the "air gap" OFETs would show lower source-drain current and a negative shift in V_T. Positive charging resulted in higher source-drain currents. This may be due to the charges remaining inside the pentacene and not being injected into the gate material layer, as shown in work by Podzorov *et al.*[34]

CONCLUSIONS

We showed that lateral OFETs can be used to visualize charge accumulation inside a gate material in a way not possible with conventional vertical devices, and that this charge accumulation is quantitatively correlated to OFET V_T shifts and influences bias stress stability. The PS can be positively or negatively charged, resulting in a V_T shift. Negative charging voltages resulted in greater V_T shifts with PS than did corresponding positive charging. PS, F-PS and PMMA show strikingly different charge penetration properties, with the polar PMMA also showing increased leakage current and the nonpolar F-PS showing superior intrinsic bias stress stability. Charging improved the bias stress stability of PS. In addition to visualizing gate material polarization and charge injection from semiconductors into

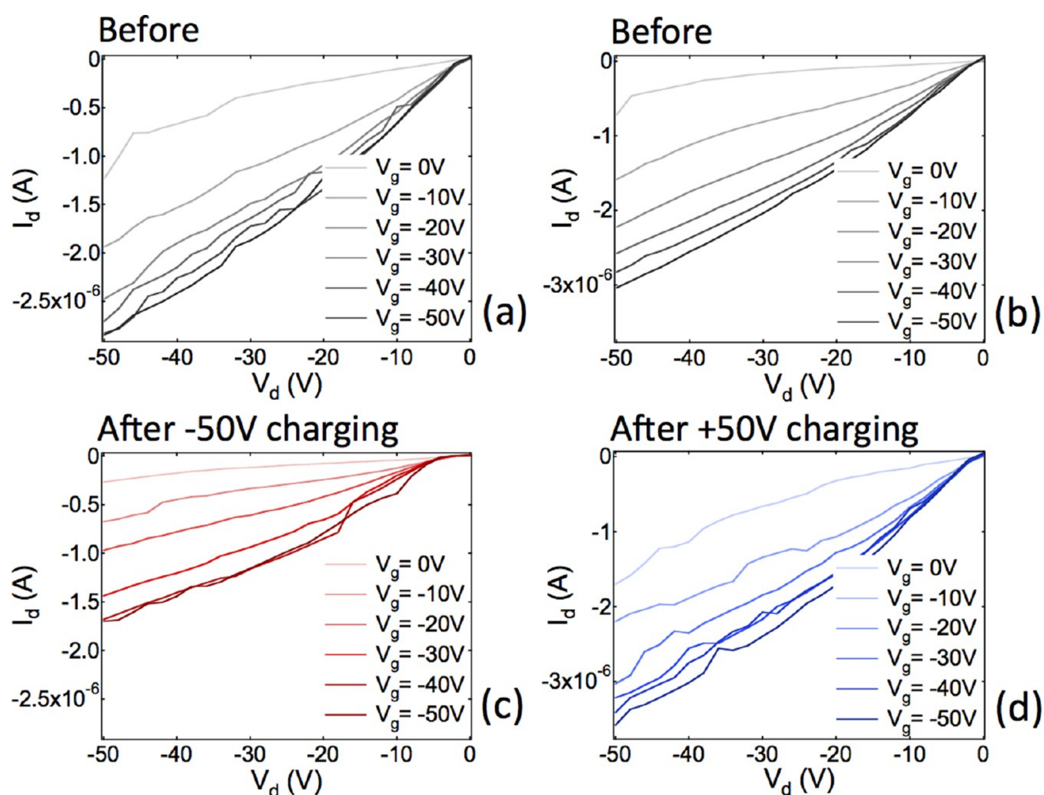


Figure 11. Output curves for lateral OFETs without a polymer gate material layer. A sample was tested before (a) and after (c) charging at −50 V for 10 min, and before (b) and after (d) charging at +50 V for 10 min. Now that the lateral OFETs have no gate material layer, the charging voltage reverses the change in output current, with the negative charging giving lower current and the positive charging giving higher current.

gate materials, this technique can be used with other combinations of materials to reveal potential differences across regions of various lateral devices during operation.

METHODS

Experimental Procedure. The bottom contact lateral OFETs were fabricated with a method very similar to one we described for our previous work, with the fabrication of the lateral transistors requiring the use of a fluorinated polymer barrier layer.[26] A schematic of the fabrication process is in the Supporting Information Figure S1. The devices were made on highly doped Si with 300 nm of thermally grown SiO_2. A 50 nm Au electrode with a 5 nm Cr adhesion layer was deposited on substrates patterned by photolithography. Atactic PS (50 000 g/mol molecular weight), F-PS, (synthesized in house and having 80 000 g/mol molecular weight) or PMMA (120 000 g/mol molecular weight) was deposited by spin coating at 2000 rpm for 1 min followed by annealing on a 95 °C hot plate for 10 min. Cytop (Asahi Glass Co.) was then deposited on top of the gate material layer by spin coating at 2000 rpm for 1 min and annealing at 95 °C for 10 min. A mask protected the portion of the polymer nearest the gate electrode, while the unprotected region was etched away with oxygen plasma (4 min at medium power). Then, 50 nm of pentacene was thermally deposited and the residual Cytop layer was removed using perfluorodecalin. After that, the underlying gate polymer between the gate electrode and the pentacene, including the interface between the polymer and pentacene, was exposed. An optical image is shown in Figure 1, along with a device schematic showing the orientation relative to SKPM scans. The OFET gate material layer was "charged" by grounding the gate electrode and applying an equal voltage to both the source and drain electrodes for 10 min. The scanning direction for each image is perpendicular to the PS−pentacene interface, from the gate to the source-drain side of the device, as shown in Figure 1(b).

Numerical Estimation of Charge Density. The potential gradient was evaluated using a 1-D central-difference method, and applied line-by-line in the same direction in which the data was collected (indicated by the double arrows in Figure 1). This approach is consistent with the line-by-line data collection of the instrument; each 2D image consists of 256 lines covering a 70 μm × 70 μm area, resulting in lateral lines spaced 273 nm apart and 273 nm between points probed along each line. As seen in Figure 2, small sparse surface contamination can contribute to abrupt changes in surface potential within one or two linescans in the image, and not representative of the entire sample. As a result, the alternative application of a 2-D gradient method, not used here, amplifies the spatial extent of these artifacts, inconsistent with the original surface potential measurement.

Small differences in the surface potential V_s are also observed near the start and end of each scan line. These differences in V_s arise from rapid changes in the tip speed near the scan edge when the tip changes scan direction. As a result, these surface potential differences manifest themselves as a band or charge density roughly 2 μm for the edge of the image on all sides. To eliminate these bands, 10 points at the start and end of each line were flattened. To identify the main topographic features in a height contour plot, each height image was contoured into 256 levels, and the area corresponding to each contour level converted into a histogram of unique height values. The three most prominent height values were selected and plotted as a height contour. These height values

roughly correspond to the Au electrodes, pentacene, and PS layers. This approach is consistent with the observation that the electrodes were evaporated simultaneously and are approximately the same height, and the PS and pentacene layers are of different height.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: A detailed description of the lateral OFET fabrication process, height profile scans of devices in the main text, SKPM scans of lateral OFETs with PMMA gate materials, and gate bias stress experiments on lateral OFETs without a PS gate material. This material is available free of charge via the Internet at http://pubs.acs.org.

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